What is claimed is:

1. A semiconductor wafer including a plurality of semiconductor chip areas, each of which includes a memory matrix, characterized in that

said each of the semiconductor chips contains a first terminal and a second terminal, the first terminal inputting a signal for judging electric connection/non-connection between a needle connected to a test apparatus at burn-in and a terminal provided in each of the semiconductor chips, and the second terminal outputting a response signal for responding to this input signal.

2. A semiconductor wafer including a plurality of semiconductor chip areas, each of which includes a memory matrix, characterized in that

said each of the semiconductor chips contains a plurality of address input terminals for specifying an address of said memory matrix;

a plurality of data input/output terminals for inputting and outputting write data and read data;

a plurality of control signal terminals for controlling write and read operations; and

a plurality of test-only signal terminals for judging electric connection/non-connection between a needle connected to a test apparatus at burn-in and a terminal provided in each of the semiconductor chips.

3. A semiconductor chip comprising:

a memory circuit containing a memory matrix; and

a test circuit inputting a signal for judging electric connection/non-connection between a needle connected to a test apparatus at burn-in and a terminal of a semiconductor chip, and outputting a response signal for responding to this input signal, and judging electric connection/non-connection between a needle connected to said test apparatus at said burn-in and a terminal of said semiconductor chip.

4. The semiconductor chip according to claim 3, wherein said test circuit comprises:

a test clock terminal for inputting a test clock signal;

a first and second test control terminals for inputting a test control signal;

a test input/output terminal for inputting and outputting test input/output data;

a first power terminal supplying with a first power supply voltage; and

a second power terminal supplying with a second power supply voltage.

5. A manufacturing method of semiconductor device in which semiconductor chips are cut out from a semiconductor wafer and a first semiconductor chip and a second semiconductor chip, separated from each other, are formed,

the method comprising a step of performing burn-in of said first and second semiconductor chips before the semiconductor chips are cut out from said semiconductor wafer.

6. The manufacturing method of semiconductor device according to claim 5, wherein said step of performing burn-in contains a step of performing a contact check for judging electric connection/non-connection between each needle connected to a test apparatus and each terminal provided in each of said first and second semiconductor chips of said semiconductor wafer.

7. The manufacturing method of semiconductor device according to claim 6, wherein said first and second semiconductor chips are cut out from semiconductor wafers different from each other.

8. The manufacturing method of semiconductor device according to claim 5, wherein said first and second semiconductor chips are cut out from semiconductor wafers different from each other.